A Primary-Side-Assisted Zero-Voltage and Zero-Current Switching Three-Level DC-DC Converter with Phase-Shift Control

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Abstract- A new primary-side-assisted zero-voltage and zero-current switching (ZVZCS) three-level DC-DC converter with phase-shift control is proposed. Three-level converters show promise for use in high-voltage applications, and ZVZCS is a very effective means for reducing switching losses. The proposed DC-DC converter uses only one auxiliary transformer and two diodes to achieve ZCS for the inner leg. It has a simple and robust structure, and offers soft-switching capability even in short-circuited conditions. The proposed converter was verified by experiments using a 6KW prototype designed for communication applications and operating at 100 kHz.

I. INTRODUCTION

Nowadays, power demand is continually increasing. The three-phase AC-DC converter operating with 380V or 440V lines is suitable as an input stage for a high-power DC-DC converter [1,2]. In the three-phase AC-DC converter, a boost power factor corrector (PFC) is widely used to comply with such regulations as the IEC61000-3-2. The primary current is to be ceased. Transformers used for aiding commutation are found in other applications [24]. Reset pulses can be provided with the circuits shown in Fig. 3. In this converter, however, there are additional losses caused by the two diodes. In Fig. 2(c) a reset pulse is supplied to the secondary side of the auxiliary transformer to absorb reactive energy when the primary current is to be ceased. Transformers for use in high-voltage applications, and ZVZCS is a very effective means for reducing switching losses.

The proposed converter has a robust structure and does not lose soft-switching capability even in short-circuited conditions or at start-up. In this converter, however, additional loss caused by the two diodes is relatively high. In Fig. 2(c) a reset pulse is supplied to the secondary side of the auxiliary transformer to absorb reactive energy when the primary current is to be ceased. The proposed converter was verified by experiments using a 6KW prototype designed for communication applications and operating at 100 kHz.

The primary-side-assisted ZVZCS converters achieve the ZCS operation by introducing resetting voltage into the primary side, which absorbs reactive energy stored in the leakage inductor [11,20-23]. A capacitor or a transformer can be used to achieve ZCS as in Fig. 2. In Fig. 2(a) the capacitor CS resets the primary current by absorbing reactive energy trapped in the leakage inductor, and the saturable inductor LS ensures the ZCS condition [20]. In this type of converter, however, an AC capacitor is needed; additionally heating of the saturable core is another serious problem. In Fig. 2(b) the capacitor CS resets the primary current by absorbing reactive energy trapped in the leakage inductor, and the two diodes ensure the ZCS condition [11,21]. In this converter, however, additional losses caused by the two diodes are relatively high. In Fig. 2(c) a reset pulse is supplied to the secondary side of the auxiliary transformer to absorb reactive energy. This circuit, however, has one drawback, that is, switch Saux is hard-switched. In Fig. 3(b) switch SA2 is closed when iL is positive, and switch SA4 is closed when iL is negative; hence, the primary voltage of TA is zero. When the reset pulse is needed, switch SA2 or SA4 is turned off and the DC input voltage VDC is reflected to the primary side to absorb the reactive energy. In this case, all the auxiliary switches SA2 and SA4 operate under ZVS condition [22]. These auxiliary switches can be merged into main switches resulting in the circuit shown in Fig. 3(c) [23].

This paper proposes a new primary-side-assisted (PA) TL ZVZCS DC-DC converter, the auxiliary circuit of which consists of only one auxiliary transformer and two diodes. The proposed converter has a robust structure and does not lose soft-switching capability even in short-circuited conditions or at start-up.
II. PROPOSED CIRCUIT

A. Operation Principle

The proposed PA ZVZCS TL DC-DC converter is shown in Fig. 4. It can be seen that the proposed converter is a combination of the circuit proposed in [8] and the primary-side auxiliary circuit illustrated in Fig. 3(c). The auxiliary circuit, including the secondary winding of the auxiliary transformer, is split into two and each is connected in parallel with its respective outer leg switch. It has three legs: an inner leg (S1 and S3), an outer leg (S2 and S4) and a passive leg (DA1 and DA3). The output power is controlled by the phase delay between the inner and outer legs. To obtain an appropriate phase delay, phase shift PWM (Pulse Width Modulation) is employed. The auxiliary circuit consists of only two diodes and a small three-winding auxiliary transformer. The primary winding of the auxiliary transformer is connected in series with the primary winding of the main transformer; two secondary windings of the auxiliary transformer are connected between the auxiliary diodes and the outer leg switches. The outer two switches operate under the ZVS condition with the assistance of reactive components C2, C4, Cfl, Lfl and Lf. The Lfl is the sum of the leakage inductances of the main transformer and the auxiliary transformer. The C2 and the C4 provide zero-voltage turn-off for switches S2 and S4. The Lfl and the Lf provide zero-voltage turn-on by changing the voltage across C4 (or C2) to E and the voltage across C2 (or C4) to zero, as well as causing the primary current to flow through freewheeling diode D22 (or D44) prior to turn on of S2 (or S4). As shown in [9], the flying capacitor (Cfl) allows phase-shift control operation. In addition, it couples C2 and C4 during transition, clamps the terminal voltage of S1 and S3, and assists with the ZVS operations of S2 and S4. The inner switches operate under the ZCS condition with the assistance of the auxiliary circuit, which provides reset voltage and absorbs reactive energy stored in leakage inductor Lfl. The passive leg operates according to the primary current; diode DA3 is turned on when i1 is positive, and diode DA1 is turned on when i1 is negative. The diodes connected in anti-parallel with the main switches are actually useless.

B. Operation Modes

Fig. 5 shows the operating waveforms; one cycle operation can be divided into five modes, and circuit diagrams of each mode are shown in Fig. 6. To simplify analysis, the magnetizing inductances of the main and auxiliary transformers are ignored, and the initial voltage across the flying capacitor is assumed to be E.

1) Model \( t_1 < t < t_2 \): During this mode, switches S1 and S4 are in conduction states and power is transferred to the load through both the main transformer and the rectifier diode Df1.
The secondary terminals of the auxiliary transformer are short-circuited by \( D_{A3} \) and \( S_4 \). Accordingly, the terminal voltage of the auxiliary transformer is zero. The current flowing through \( S_4 \) is given by

\[
i_{s4} = \left( 1 + \frac{1}{n_2} \right) i_1.
\]  

(1)

2) **Mode 2** \((t_2 < t < t_4)\): This mode is initiated by turning off \( S_4 \). A resonant circuit is constructed with \( C_2 \), \( C_4 \), \( C_{fl} \), \( L_{lk} \) and \( L_f \). The \( C_p \) couples \( C_2 \) and \( C_4 \) and assists with the zero-voltage turn-on of \( S_2 \). The equivalent circuit is shown in Fig. 6(f). The voltage across capacitor \( C_2 \) is given by

\[
v_{c2} = E - n_2 V_{aux}(1 - \cos \omega_c (t - t_2)) + I_1(t_2) C_eq \sin \omega_c (t - t_2),
\]  

and the primary current \( i_1 \) is given by

\[
i_1 = \frac{E - n_2 V_{aux}}{Z_o} \sin \omega_c (t - t_2) + I_1(t_2) \cos \omega_c (t - t_2),
\]  

where

\[
\omega_o = \frac{1}{\sqrt{L_eq C_eq}},
\]  

(4)

\[
Z_o = \frac{L_eq}{\sqrt{C_eq}},
\]  

(5)

\[
L_eq = L_{lk} + n_1^2 L_f,
\]  

(6)

\[
C_eq = \left( C + \frac{C_{fl}}{C + C_p} \right) \left( \frac{n_2}{1 + n_2} \right)^2,
\]  

(7)

\[
C = C_2 = C_4.
\]  

(8)

The voltage across the capacitor \( C_2 \) is given by

\[
v_{c2} = E - \frac{C_p}{C + C_p} v_{c4}.
\]  

(9)

The primary current \( i_1 \) is nearly constant during this interval, since \( n_1^2 L_f \) is large and this interval is short. The voltage across \( S_4 \) increases smoothly to \( E \), which results in zero-voltage turn-off of \( S_4 \).

3) **Mode 3** \((t_3 < t < t_4)\): This mode is initiated after the voltage across \( S_4 \) reaches \( E \), and the primary current flows through \( D_{22} \). Half of the input voltage is introduced to the secondary winding of the auxiliary transformer and reflected to the primary one, as shown in Fig. 6(c). The reactive energy trapped in inductor \( L_{lk} \) is recovered to the DC side. The primary current \( i_1 \) decreases to zero as

\[
i_1 = I_1(t_3) - \frac{V_{aux}}{L_{ik}} (t - t_3),
\]  

(10)

where \( V_{aux} \) is the reflected voltage of the input DC side through the auxiliary transformer, acting to reset the primary current, and which is given by

\[
V_{aux} = \frac{E}{n_2}.
\]  

(11)

Assuming \( C << C_p \), equation 9 determines that

\[
v_{c4} = 0.
\]  

(12)

Hence, \( S_2 \) can be turned on with ZVS condition, which leads to the conclusion that \( C_p \) should be sufficiently large to ensure ZVS.

4) **Mode 4** \((t_4 < t < t_5)\): This mode is initiated after the primary current becomes zero. During this mode the primary current remains at zero, and the load current flows evenly through \( D_{fl} \) and \( D_{f2} \), as shown in Fig. 6(d). Also in this mode, switch \( S_t \) is turned off with ZCS condition.

5) **Mode 5** \((t_5 < t < t_6)\): This mode is initiated by turning on switch \( S_3 \) with ZCS condition. The primary current \( i_1 \) begins to flow through switches \( S_2 \) and \( S_3 \). The secondary terminals of the auxiliary transformer are short-circuited by \( D_{A3} \) and \( S_4 \). The primary current \( i_1 \) is given by

\[
i_1 = \frac{E}{L_{ik}} (t - t_3).
\]  

(13)

The load current flowing through \( D_{fl} \) is diverted to \( D_{f2} \) as \( i_1 \) increases. This mode ends when the current flowing through \( D_{fl} \) becomes zero.

In this way, one switching cycle is completed. The next switching cycle begins with Mode 1, during which switches \( S_2 \) and \( S_3 \) are in conduction states.

![Fig. 5. The operational waveforms of the proposed circuit.](image-url)
Fig. 6. Operating modes of the proposed circuit:
(a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; and (f) equivalent circuit for Mode 2.
C. Conditions for ZVZCS Operation

The zero-voltage turn-off of switch $S_4$ is natural, as $C_{eq}$ is connected in parallel with $S_4$. In a full-bridge DC-DC converter, if $v_{C4}$ reaches the level of the DC-link voltage, the safe zero-voltage turn-on of $S_2$ can be attained. In this three-level DC-DC converter, however, one more condition is needed because although $v_{C4}$ reaches $E$ at the end of mode 2, $v_{C2}$ is not exactly zero. Its final voltage depends on the ratio of $C_β$ to $C$. To achieve safe ZVS-on of $S_2$, the final voltage of $v_{C2}$ must be less than the on-voltage of the switch. The extra condition is given by

$$C_β > C\left(\frac{E}{V_s} - 1\right).$$

where $V_s$ is the on-voltage of the switch.

The primary current $i_1$ is nearly constant during mode 2, since $n_1^2L_f$ is large and the time interval is short. The time interval given to switches $S_1$ and $S_2$ for ZVS operation is given by equation 15, and is easily designed by selecting the appropriate $C_{eq}$. Accordingly, the rate of change of the voltage across the outgoing switch is adjustable, as follows:

$$T_{ZVS} = T_s - T_l = \frac{C_βE}{I_1}.$$

During mode 3, zero-current turn-off operation in the inner switches is accomplished by eliminating the primary current prior to removing the gate pulse of $S_1$. The approximate time interval required to eliminate the primary current is given by

$$T_{ZCS} = T_s - T_l = \frac{L_{eq}I_1}{V_{max}}.$$

This ZCS operation does not depend on the output voltage, and can be achieved regardless of the output voltage if the DC-link voltage is established. The $T_{ZCS}$ is at its maximum when the current is at its maximum, and the maximum $T_{ZCS}$ is given by

$$T_{ZCS max} = \frac{L_{eq}I_{max}}{V_{max}},$$

where $I_{max}$ is the maximum primary current allowed. The condition for safe ZCS operation is given by

$$T_{ZCS max} < (1 - D_{max})T_s,$$

where $D_{max}$ is the maximum duty cycle and $T_s$ is the switching period.

D. Additional Conduction Losses in ZVZCS Converters

All ZVZCS converters adopt auxiliary circuits to achieve ZCS. The auxiliary circuits, however, cause additional losses. In welding applications for which the duty cycle is about 0.3–0.6, the additional losses are relatively small compared to the freewheeling conduction loss. In communication applications, the conduction loss sometimes exceeds the freewheeling conduction loss of the ZVS converter since the duty cycle is about 0.7–0.9. So it is very important to understand how the losses are produced.

Such reactive components as the capacitor, saturable reactor and coupled inductor or transformer are usually considered to consume insignificant powers. However, losses in these reactive components are not negligible when the converters operate at high frequencies. Saturable reactors [12, 20] in particular are usually not recommended because their losses are relatively high and heats are also problematic.

Hard-switched active devices are also not recommended [9,13]. The diode is the device most commonly used. The amount of current that the diode carries determines the additional conduction loss. In PA ZVZCS converters, the diode is assumed to have the same on-voltage as the active switches, and in SA converters the auxiliary diode is assumed to have the same on-voltage as the main rectifier diodes. If the on-voltages are different, the on-voltage ratio may be multiplied. Some previous works [11] and [21] have had high additional conduction losses even though on-voltage ratio is taken into account. They will reach 20–50% primary conduction loss, which exceeded the freewheeling losses.

To achieve ZCS in SA ZVZCS converters, the peak discharging current of the auxiliary circuit must be equal to or greater than the maximum load current. However, the average discharging current (I_{dis}) is different from circuit to circuit. [16] and [17] have large average discharging currents because they use lowered capacitor voltages with large capacitances.

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Additional Loss</th>
<th>Circuit Type</th>
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<tbody>
<tr>
<td>PA ZVZCS</td>
<td>$\frac{V_s}{n_1}$</td>
<td>[11],[21]</td>
</tr>
<tr>
<td>SA ZVZCS</td>
<td>$2I_{dis}/I$</td>
<td>[16],[17],[19]</td>
</tr>
<tr>
<td></td>
<td>$3I_{dis}/I$</td>
<td>[15]</td>
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</tbody>
</table>

E. Conduction Loss and Limitation of the Proposed Circuit

The additional loss in the proposed circuit and the reduction of freewheeling loss depend on $n_2$ so we can optimize loss by a appropriate $n_2$. Combining equations 11, 17 and 18 determines the range of $n_2$ such that the reset voltage ensures ZCS operation, as follows:

$$n_2 < \frac{2\pi(1 - D_{max})}{\%Z_{fl}}.$$

where $\omega$ is the switching angular frequency and

$$\%Z_{fl} = \frac{\omega L_{eq}I_1}{E}.$$

In a case of low duty cycle, the ratio of the turns of the auxiliary transformer is decided within the range given in equation 19 such that the conduction loss may be minimized. Assuming that the primary-side switches have the same on-
voltage, the respective conduction losses of the ZVS and ZVZCS DC-DC converters can be obtained as follows:

\[ P_{\text{lossZVS}} = 2V_i I_1, \text{ and} \]

\[ P_{\text{lossZVZCS}} = 2V_i I_1 \left(1 + \frac{1}{n_2^2}\right)D + V_i I_n\left(1 + n_2\right)\frac{\%Z_{in}}{2\pi}, \]  

(22)

where \( V_i \) is the on-voltage of the switches, and \( D \) is the duty cycle.

In equation 22, the power loss in the ZVZCS converter is minimized when \( n_2 \) is set as in equation 23:

\[ n_2 = 2\sqrt{\frac{\pi D}{\%Z_{in}}}. \]  

(23)

From equations 18 and 23, the range of \( D \) can be obtained such that the conduction loss in the ZVZCS converter does not become higher than that of the ZVS converter, as given by

\[ D < \left(1 - \frac{1}{2}\sqrt{\frac{\%Z_{in}}{\pi}}\right)^2. \]  

(24)

**III. EXPERIMENTAL RESULTS**

A 6KW prototype of the proposed circuit was constructed and tested. It was designed for use in communication applications. The normal operating voltage is 800 V, and the final voltage at holdup time is 660 V. The operating frequency is 100 kHz and the switching frequency is 200 kHz. Circuit parameters and components used are shown in Table 2; results are shown in Figs. 7 ~ 10. Fig. 7 shows the measured efficiency curve. Maximum efficiency is about 95.5%. In Fig. 8 the top trace is the bridge output voltage \( v_{AB} \); the middle trace is the voltage \( v_{BC} \) of the secondary winding of the auxiliary transformer; and the bottom trace is the primary current of the main transformer. It can be seen that the two DC-link voltages are balanced, the inner switches operate in ZCS mode, and the reset voltage is introduced during mode 3 and disappears when the primary current is reduced to zero. Fig. 9 shows the drain-to-source voltage and gate signal of an outer switch. It can be seen that the voltage falls to zero prior to the turn-on of the gate signal, which means ZVS operation is achieved. Fig. 10 shows the operation under the short-circuit condition; the output terminal is shorted with 0.022 ohm wire and the output current is 90A. From this, we can see that the ZCS operation is guaranteed even when the output terminals are shorted.

<table>
<thead>
<tr>
<th>Table 2. Components and Parameters Used</th>
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<tr>
<td>( S_1, S_2 )</td>
</tr>
<tr>
<td>( D_{1}, D_{2} )</td>
</tr>
<tr>
<td>( D_{3}, D_{4} )</td>
</tr>
<tr>
<td>( D_{5}, D_{6} )</td>
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IV. CONCLUSION

A new PA ZVZCS TL DC-DC converter with phase-shift control is proposed. Three-level converters show promise for use in high-voltage applications, and ZVZCS is a very effective means for reducing switching losses. The proposed DC-DC converter uses only one auxiliary transformer and two diodes to achieve ZCS for the inner leg. It does not lose soft-switching capability at start-up or at short-circuited load. The operation of the converter is verified by experiments using a 6kW prototype operating at 100 kHz. Due to its simplicity and robustness, the proposed topology is thought to be suitable for high-voltage and high-power applications.

REFERENCES


