A PFC Boost Converter with Lossless Snubber under Minimum Voltage Stress*

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Abstract—A passive lossless turn-on/turn-off snubber network is proposed for the boost PWM converter. Besides the benefit of small number of added components, all the devices block the voltage no more than the output DC voltage. The operation principle and design guideline is presented. Experimental results demonstrate that for 1 kW PFC AC/DC boost converter, the proposed snubber circuit can achieve significant efficiency improvement over the hard-switching converter.

I. INTRODUCTION

Many snubber techniques have been proposed to improve the switching performance of the continuous-conduction-mode (CCM) boost converter. The main reason stems from the fact the CCM boost converter is a popular topology for use in front-end converter with an active power-factor-correction (PFC) function, which is usually used in the distributed power systems (DPS) of the server and telecommunication applications.

Among those techniques, the active snubbers, as introduced in previous work [1], can reduce both the turn-on and turn-off losses of the main devices by employing the auxiliary active switch. However, the auxiliary switch needs to be operated under the hard turn-off condition, which unfortunately offsets the loss reduction from the main switch. Although some active snubber techniques [2]-[3] can achieve soft switching (including the snubbed turn-off) for both the main and the auxiliary switches, the complexity of the power and control circuit usually prevents their use in the front-end PFC circuit. In the interest of simplicity, other works have proposed the use of the active snubber circuits to solve only the turn-on losses caused by the diode reverse recovery [4]-[5].

To effectively reduce the cost and complexity, passive snubbers are also presented for use in the boost converter. Passive snubber techniques using only the non-coupled inductors have been reported [6]-[8]. Those techniques normally require a relatively high number of extra components since the turn-on and turn-off operations are achieved by different sets of auxiliary circuit networks. Others have attempted to achieve great simplicity with the passive snubber techniques that use the inductors coupled with the main boost inductor [9]-[12].

One passive snubber circuit [9] makes use of the reflected voltage of the coupled inductor to completely transfer the secondary current to the output diode during the switch’s off period. As a result, upon the switch’s turn-on, one inductor is always put in series with both the switch and the output diode. Using the series inductor to slow the di/dt reduces the reverse recovery charge and thereby the turn-on loss. On the other hand, the snubber capacitor is added to reduce turn-off loss of the switch. The snubber capacitor’s discharge is realized via an additional inductor, which is independent from the coupled inductors intended for turn-on loss reduction. The penalty of this technique is the rather complicated power stage that results from the high component counts. While another technique also uses one coupled inductor, it serves the purpose of discharging the snubber capacitor instead of being involved in the turn-on snubber function [10].

Another passive snubber technique [11]-[12] generalizes and extends the coupled inductor concept to realize the turn-on snubbing function. The coupled winding of the main boost inductor is used to shift the original output diode current to an alternative branch during the switch’s off period. This alternative branch has one inductor or leakage inductor in series with the auxiliary output diode. Consequently, the inductor will slow the di/dt upon the turn-on of the switch, thus decreasing the turn-on loss related to diode reverse recovery. This approach has the lowest component counts as compared with the two methods previously discussed. However, it only achieves the turn-on snubber function by suppressing the diode reverse-recovery current. The device is still turn-off under the hard-switching condition.

Besides, due to the inductor placement, one common issue for these boost converters [9]-[12] is a severe, undesirable resonance between the output capacitance of either active switch or diode and the equivalent resonant inductor. The ringing causes excessive voltage stress over the semiconductor devices and affects the circuit operation. An extra clamping circuit is mandatory to protect the devices in practical implementation. For example, one extra capacitor together with two series diodes or the R-C-D snubber forms the clamping circuit to protect the auxiliary output diode [11]. This paper proposes a new lossless snubber configuration for the boost converter. It further enhances the previously developed concept of turn-on and turn-off snubber function developed in [9]-[12]. One coupled inductor is used to help

*This work made use of ERC Shared Facilities supported by the National Science Foundation under Award Number EEC-9731677.

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reduce both the turn-on and the turn-off losses. During the switch’s off period, the coupled inductor shifts the current from the original output diode to the auxiliary output diode. Therefore, the diode reverse recovery loss is greatly reduced, comparable to that achieved in other work [10]-[11]. After the switch is on, the coupled inductor can charge the snubber capacitor voltage to the output voltage level. Consequently, the diode reverse recovery loss is greatly reduced, comparable to that achieved in other work [10]-[11]. After the switch is on, the coupled inductor can charge the snubber capacitor voltage to the output voltage level. Consequently, the snubber capacitor can effectively slow the voltage rising rate at the switch’s turn-off, and can reduce the turn-off loss accordingly. The reduced dv/dt is also expected to alleviate the electromagnetic interference (EMI) noise. The proposed snubber circuit has two interesting features: All devices prevent the voltage from surpassing $V_o$, and no additional clamping circuit is required in the actual implementation; the circuit requires only a small number of added components, one coupled inductor, three auxiliary diodes and one snubber capacitor. Although there is one more diode voltage drop during the switch’s off period as compared with the conventional hard-switching boost converter, the resultant extra conduction loss is not significant when compared with the switching loss reduction.

II. PRINCIPLE OF OPERATION

The circuit diagram of the boost converter incorporating with the proposed snubber circuit is shown in Fig. 1. The turn-on/off snubber circuit is composed of three diodes, $D_s$, $D_c$ and $D_a$, one coupled inductor, and one snubber capacitor $C_s$. Primary winding $N_1$ serves as the boost inductor of the conventional boost converter when switch $S$ is on. Three extra diodes and the original output diode $D_o$ together form one full-bridge-like diode clamping network, which has secondary winding $N_2$ across the junction point of each pair of series-connected diodes. Snubber capacitor $C_s$ is in parallel with diode $D_s$.

For the convenience of explanation, the coupled inductor is regarded as a combination of the magnetizing inductor $L_m$, an ideal transformer with the turns ratio $1 : n$ ($n>1$), and a leakage inductor $L_k$, as shown in Fig. 2, which also shows the reference direction of the voltages and currents. To facilitate the explanation of the circuit operation, magnetizing current $I_{lm}$ serves as the boost inductor of the conventional boost converter when switch $S$ is on. Three extra diodes and the original output diode $D_o$ together form one full-bridge-like diode clamping network, which has secondary winding $N_2$ across the junction point of each pair of series-connected diodes. Snubber capacitor $C_s$ is in parallel with diode $D_s$.

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[Before $T_0$]: The circuit is in the normal switch conduction mode and the switch $S$ carries the constant $I_{lm}$.

[$T_0$, $T_1$]: At $T_0$, switch $S$ is turned off. The magnetizing current is shifted from $S$ to the branch of $D_o$ and $D_s$. Compared with the hard-switching case, the rising rate of $V_s$ is slowed down due to the snubber capacitor. Assuming the initial voltage of $C_s$ is $V_o$, the rising rate is given as follows:

$$\frac{dV_s}{dt} = \frac{I_{lm}}{C_s}. \tag{1}$$

Therefore, the overlap of the switch current and voltage is reduced, and the turn-off loss is thus decreased by the snubber capacitor.

[$T_1$, $T_2$]: The current-shifting process, from output diode $D_o$ to alternative diode $D_a$, begins in this period. At $T_1$, $D_a$ starts to conduct the whole load current when $V_{Cs}$ drops to zero. Since the turns ratio $n$ is designed to be slightly larger than one, the reflected secondary winding voltage is higher than the primary winding voltage. As a result, the positive voltage is applied to secondary leakage inductor $L_k$ and linearly builds the current of $L_k$, the same as the current of $D_a$, at the rate expressed by the following:

$$\frac{di_{Lk}}{dt} = \frac{(n-1)(V_o - V_{mi})}{L_k}. \tag{2}$$

When $i_{Lk}$ is increased, the primary winding current of the ideal transformer is also increased and flows out of the dotted end. Therefore, $i_{Lp}$ is decreased, and thus the $D_o$ current decreases.

At $T_2$, $i_{Lp}$ reaches zero and $D_o$ ceases conduction. Consequently, the current of $D_s$ becomes the same as $i_{Lk}$. The level of $i_{Lk}$ at $T_2$ is given as follows:

$$i_{Lk} (t_2) = \frac{I_{lm}}{n}. \tag{3}$$

Thus it is easy to derive that the time for the primary winding current to decrease to zero, $T_{shift}$, is equal to $T_2-T_1$, as described in (4):

$$T_{shift} = T_2 - T_1 = \frac{L_k I_{lm}}{n(n-1)(V_o - V_{mi})}. \tag{4}$$
Fig. 3. Topological modes within one switching cycle; (a) [before T_1], (b) [T_1, T_2], (c) [T_2, T_3], (d) [T_3, T_4], (e) [T_4, T_5], (f) [T_5, T_6], (g) [T_6, T_7], (h) mode in [T_7, T_8].

[T_2, T_3]: Diode D_o naturally recovers after T_2. It blocks a small level of voltage so that the net voltage applied to L_k is almost zero. The current equal to I_{Lm/n} flows to the output through the path comprised of D_o, L_k and D_a.

[T_3, T_4]: At T_3, switch S is turned on by the gate signal, and its voltage quickly drops to zero. The input voltage V_in is applied to the primary winding and the reflected secondary voltage is nV_in. Therefore, the current of L_k is forced to reduce at the rate given by (5):

\[
\frac{di_{L_k}}{dt} = \frac{V_o + (n-1)V_{in}}{L_k}.
\]  

So I_{Lm} increases at the rate which is 1/n times the rate at which i_{Lk} decreases. The primary winding current flows into S. Within this period, D_o blocks output voltage V_o since the voltage of S is zero.

[T_4, T_5]: At T_4, the current of L_k reaches zero and continues to progress towards negative direction due to the reverse-recovery of D_a. D_s does not need to block the voltage because D_o blocks V_o. Since L_k limits the di/dt of the D_a current, the reverse-recovery current peak is dramatically reduced compared with the hard-switching condition. The reflected reverse-recovery current appears on the current of S.

[T_5, T_6]: At T_5, the reverse-recovery current reaches its peak value. Diode D_a starts to block the voltage of V_o-V_in. The reflected secondary voltage, nV_in, makes the diode D_c conduct and then charges the resonant network of L_k and C_s. The maximum voltage of C_s to be charged is about 2nV_in if the reverse recovery current is considered to be very small. This implies that the condition for the full snubber turn-off is V_{in} < V_o/2n. Since the input voltage varies over the line cycle in the PFC application, the voltage level of C_s prior to turn-off varies accordingly.

Under the unity power factor, the higher the instantaneous input voltage, the higher the input current. It is somewhat desirable for the C_s voltage prior to the switch’s turn-off to follow the input AC voltage. Since the voltage rising rate at the turn-off is determined by the instantaneous load current, as indicated in (1), the unchanging level V_o of the snubber capacitor C_s will lead to an excessively long turn-off transition time in the region of low input current. This expanded duration causes input current distortion and would...
deteriorate the power factor. On the other hand, the turn-off loss depends heavily on the instantaneous input current level. Turn-off loss at small input current is rather small. Incomplete turn-off snubber function at the small input current will not largely affect the overall turn-off loss reduction for the converter.

The peak current of \( D_s \) is given by (6):

\[
I_{Dc(pk)} = \frac{nV_in}{Z} - \frac{nV_in}{\sqrt{L_k/C_s}}.
\]

The current of \( D_c \) is reflected into switch S. The added current peak above the \( I_{in} \) is given by (7):

\[
\Delta I = nI_{Dc(pk)} = \frac{n^2V_in}{\sqrt{L_k/C_s}}.
\]

If \( V_{in} = V_{in}/2n \), the corresponding circuit is shown in Fig. 3(g). At \( T_6 \), the current of \( L_k \) almost reaches zero. The waveform in Fig. 4 explains the case when \( V_{in} = V_{in}/2n \). Under such conditions, \( V_c \) reaches \( V_o \) at \( T_6 \). If \( V_{in} > V_{in}/2n \), the equivalent circuit is shown in Fig. 3(h), which means that when \( C_s \) is charged to \( V_o \) at \( T_6 \), the current of \( L_k \) remains low. Then, \( L_k \) is discharged toward zero by output voltage \( V_o \) through diode \( D_c \) and \( D_o \).

[After \( T_6 \): The circuit resumes the operation indicated in Fig. 3(a). \( D_c \) blocks voltage \( V_o - nV_in \) and \( D_o \) blocks voltage \( (n-1)V_in \). S conducts magnetizing current \( I_{in} \).

It is interesting to note that \( D_o \) is the major diode, which undergoes the reverse recovery after S turns on at \( T_3 \). From the previous analysis, \( D_o \) only needs to block \( V_o - V_{in} \). Under the hard-switching condition, the output diode \( D_o \) must block \( V_o \). In the snubber circuit, after its current reaches zero, \( D_c \) does not need to block voltage immediately since \( D_o \) has already blocked \( V_o \). The proposed snubber circuit not only reduces the di/dt that results from the diode’s turn-off but also lowers the blocking voltage level after the diode’s recovery. Therefore, the proposed snubber circuit should dramatically reduce both the switch’s turn-on loss and the diode’s turn-off loss.

It also needs to be mentioned that the additional diode voltage drop as compared to the number in the hard-switching converter in the switch’s off period does not necessarily double the output diode’s conduction loss. The preceding analysis has indicated that the \( D_o \) in the snubber circuit is not required to be a hyper-fast recovery diode since it need not immediately withstand the output voltage after carrying the load current. Furthermore, the conduction loss in the output diode of the boost converter is inherently small due to the high output voltage level. Thus the extra conduction loss that occurs due to the two series output diodes is justified by the significant reduction in the turn-on and turn-off losses.

### III. Design Guideline and Example

The design objectives are listed below.

1. Minimize the switching loss.
2. Ensure a short switching transition time within the load and duty cycle range.
3. Minimize the added current peak of the main switch.

The basic design idea is straightforward. First, \( C_s \) should be selected such that it ensures the optimum turn-off loss reduction. Second, \( L_k \) and the turns ratio \( n \) should guarantee the significant turn-on loss reduction. Third, the potential duty cycle loss and the peak current of the switch should be determined. Should be unsatisfied, \( C_s \) or \( L_k \) should be lowered and the design procedure should be repeated. The extra peak current in the switch should be checked for the sake of EMI noise rather than the current stress. Usually, the MOSFET device has superior peak current handling capability. The following example uses the universal-line input 1kW PFC circuit to illustrate the design philosophy. Two MOSFET IRF460s in parallel are selected as the main switch. The \( V_o \) is chosen as 400 V, and the switching frequency \( f_s \) is 100 kHz.

- **Step I:** Select the proper snubber capacitance \( C_s \).
  - Generally, a larger \( C_s \) leads to a smaller turn-off loss. Previous work has found that when the snubber capacitor is above a certain value, no further loss reduction is observed [7]. One practical rule for selecting \( C_s \) is given by (8):

\[
C_{s(opt)} = \frac{I_{R_s}C_{dg}}{V_{plateau}^2},
\]

where

- \( I_s \) is the switched current at turn-off,
- \( R_s \) is the gate resistor when using the voltage source,
- \( C_{dg} \) is the drain to gate capacitance of the MOSFET device, and
- \( V_{plateau} \) is the gate plateau voltage.

The maximum switched current \( I_s \) is about 15 A. For the IRFP460, \( R_{s}=5 \Omega, C_{dg}=100 \mu F, \) and \( V_{plateau}=4.2 \) V. According to (8), \( C_{s(opt)}=2 \) nF.

- **Step II:** Design the leakage inductance \( L_k \) and turns ratio \( n \).
  - To effectively suppress the diode reverse recovery-related loss, two conditions should be satisfied. First, the current decreasing rate at \( D_o \)’s turn-off should generally be no more than 100 A/μS. Assuming \( n \) is close to one, it is known from (5) that \( L_k >= 4 \) μH. Second, the primary winding current needs to definitely able to shift the branch of \( D_o \) during the switch’s off period. In other words, the following is valid:

\[
T_{shut} < (1 - D)T_s = \frac{V_{in}}{D_oT_s}.
\]

where

- \( D \) is the duty cycle, and
- \( T_s \) is the switching period, equal to \( 1/f_s \). Substituting (4) into (8), the following expression determines the turns ratio,

\[
n > \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{V_o}{V_{in}} L_m k_s f_s},
\]

For the PFC application, the input voltage is the AC voltage, and can be expressed by

\[
V_{in} = V_{in(pk)} \sin(wt),
\]

where

- \( V_{in(pk)} \) is the peak value of the input AC voltage, and
- \( w \) is the angular frequency of the input AC voltage.
Since $I_{Lm}$ is almost the same as the input current, it is expressed by 

$$I_{Lm}(t) = I_{in(pk)}\sin(wt) = \frac{2P_o\sin(wt)}{V_{in(pk)}}\ ,$$  \hspace{1cm} (12)

where $P_o$ is the output power.

Substituting (11) and (12) into (10), the turns ratio is obtained by

$$n > \frac{1}{2} + \frac{1}{4} \left(1 + \sqrt{1 + \frac{V_o^2 P_o L_k f_s}{V_{in(pk)}^2 (V_o - V_{in(pk)} \sin(wt))}}\right) .$$  \hspace{1cm} (13)

Based on (13), the design curves for selecting the turns ratio $n$ is plotted in Fig. 5. $L_k=4 \mu H$ is chosen to obtain a $dV/dt$ of 100A/$\mu S$. Then the turns ratio $n$ is designed to be 1.07.

Step III: Check whether the duty cycle limit and current peak are acceptable.

The current rising rate in the switch at turn-on is $1/n$ times the falling rate of $I_{Lk}$. For 1 kW of output power, the time for the switch current to rise to the maximum input current is calculated from (5). The designed parameters result in 146 nS, which is negligible in relation to the switching period of 10 $\mu S$. The resonant charging time of the snubber capacitor is expressed by

$$T_s = \pi \sqrt{L_k C_s} .$$  \hspace{1cm} (14)

So, $T_s$ is about 280 nS. The maximum total turn-on time is 426 nS, which will not severely limit the duty cycle. Since the $C_s$ voltage is adjusted according to the input voltage, the turn-off transition time is usually not an issue.

Besides the duty cycle limitation check, the added current peak $\Delta I$ during the switch turn-on is also derived from (7). Fig. 6 shows the $\Delta I$ change over $L_k$ at different input line voltages. For 90 V$_{ac}$ input, the added peak current at the line peak voltage is around 3 A. Therefore, the designed parameters are acceptable. To further optimize the design, the quantitative trade-off among the loss, the EMI and the duty cycle loss must be required. However, this is outside the scope of this paper.

IV. EXPERIMENTAL VERIFICATION

Based on the designed parameters, one prototype PFC circuit for the universal-line input is constructed as shown in

Fig. 7. The same PFC controller (based on the ML4821) is used to generate the PWM signals for both the snubber circuit and the hard-switching circuit. When operated under the hard-switching mode, $D_o$ is used as the output diode.

Figure 8 demonstrates the unity power factor achieved by the proposed snubber circuit. Key operating waveforms at 110 V$_{ac}$ of input are shown in Fig. 9. Figure 9(a) and (b) show the relationship between $V_{ds}$, $V_{cs}$, $I_{Lp}$ and $I_{Lk}$. Before the switch turns off, the snubber capacitor has been charged to a voltage level of 2$nV_{in}$. The magnetizing current discharges $C_s$ during the turn-off. Therefore, the switch is under the snubbed turn-off condition. Following each s turn-on, $C_s$ is

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**Figures and Captions**

1. **Fig. 5.** Relationship of designed turns ratio and the leakage inductance.
2. **Fig. 6.** Maximum value of additional current peak at turn-on with $C_s=2$ nF.
3. **Fig. 7.** Experimental circuit configuration for 1 kW PFC operation.
4. **Fig. 8.** Input voltage and current waveforms at 90 Vac input.
subsequently charged again, preparing the voltage for turn-off. The charging and discharging process of \( C_s \) is clearly seen in Fig. 9(a). In the test waveforms, \( C_s \) is first charged to about 320 V and then settles at 260 V. The junction capacitance of \( D_o \) and \( C_s \) is considered to be composed of one voltage divider, which affects the final voltage distribution on \( C_s \). The turn-on snubber function is also verified in Fig. 9(b). Before \( S \)'s turn-on, the primary winding current is completely

“shifted” to the secondary side. As a result, the leakage inductance at the secondary side can limit the diode reverse-recovery current. The added current in the switch corresponds to the reflected charging current of \( C_s \). The closed view of the turn-on process, as shown in Fig. 9(c) indicates a very small

![Fig. 9. Test results of the switch voltage \( V_{ds} \), the snubber capacitor voltage \( V_{Cs} \), the primary winding current \( I_{Lp} \) and secondary winding current \( I_{Lk} \). (a) turn-off snubber function, (b) turn-on snubber function, (c) zoomed turn-on.](image)

![Fig. 10. Detailed diode voltage waveforms during the recovery at switch turn-on: (a) \( D_a \) only needs to block \( V_o-V_{in} \), and (b) \( D_o \) blocks \( V_o \) during turn-on.](image)

![Fig. 11. Efficiency comparison between the snubber and hard-switching CCM PFC boost converter at \( f_s=100 \) kHz and \( P_o=1 \) kW.](image)
overlap between the switch voltage and current, which means there is only a small amount of turn-on loss. It is estimated from the waveforms that the dI/dt of the switch current at turn-on is 110 A/µS, which roughly matches the design projection.

As pointed out in Section II, in the proposed snubber circuit the fast recovery diode D_a in the alternative branch only needs to block V_o-V_in. As shown in Fig. 10(a), including the effect of the parasitic in the circuit, D_a blocks no more than 300 V after turning off at high current. D_o, with no current flowing before turning on the switch, quickly blocks the output voltage V_o when the switch turns on, as can been from Fig. 10(b). After D_a has almost recovered, the D_o voltage begins to slowly decrease. This implies D_a has began to block voltage. Therefore, the D_a’s series diode, D_o does not need to be hyper-fast, which helps to further alleviate any extra conduction loss.

Figure 11 compares the efficiency performance of the snubber circuit and the hard-switching CCM boost converter at f_s=100 kHz. The proposed snubber circuit can operate at the low line, 90 Vac, without any thermal problems. The hard-switching converter can deliver full power only at the input-line voltage, which is no less than 115 V_ac. At 115 V_ac, thermal runaway of the hard-switching converter occurs. The temperature of MOSFET’s heat sink is higher than 75 °C at 115 V_ac of input while in the snubber circuit the temperature of the MOSFET’s heat sink is 63 °C even at 90 V_ac. This indicates the switching losses of the snubber circuit’s MOSFET are dramatically reduced compared with those resulting from the hard-switching operation. The efficiency measurement does not intend to give a absolute data instead focus on the relative performance comparison. The proposed snubber circuit achieves 1.5% efficiency improvement at 115 V_ac, which translates into about 17 W of loss savings. It is concluded that the snubber circuit can extend the converter’s input voltage range without de-rating the output power.

V. SUMMARY

The new turn-on/off snubber circuit for the PFC boost converter is described in this paper. The theoretical operation principle and the design guidelines are presented. Based on the design guidelines, the snubber circuit is implemented at a 1kW PFC boost converter. The experimental results verify the validity of the operation principle and demonstrate that the new snubber circuit can effectively improve the converter efficiency and significantly extend the input voltage range. The proposed snubber circuit is a cost-effective technique for applications involving the PFC boost converter with universal-line input.

REFERENCES